

**A 4-bit Uncontrolled Buffer Register**

**Note: Coding same as for controlled one just remove load input from controlled design to become uncontrolled.**

**moduleubr (CK, DIN, Q);**

**input CK;**

**input [7:0] DIN;**

**output [7:0] Q;**

**reg [7:0] Q;**

**always @ (posedge CK)**

**Q <= DIN;**

**endmodule**

**moduletest\_ubr;**

**reg CK;**

**reg [7:0] DIN;**

**wire [7:0] Q;**

**ubr r1 (CK, DIN, Q);**

**always**

**#3 CK = ~CK;**

**initial**

**begin**

**CK = 0;**

**#5 DIN = 8'b10101010;**

**#8 DIN = 8'b11110000;**

**#17 DIN = 8'b00001111;**

**end**

**endmodule**